Materials for Integrated Circuits

Question:- Discuss CMOS working Principle and applications. Also give an overview of the process sequence for fabrication of CMOS integrated circuit.

Solution:- CMOS working Principle:-

In cmos technology, both N-type and P-type transistors are used to design logic function The same signal which turns ON a transistor of one type is used to turn Off a transistor of the other type. This characteristic allows the design of logic devices using only simple switches, without the need for a pull-up resistor.

In CMOS logic gates a collection of N-type MOSFETS is arranged in a pull-down network between the output and the low voltage power supply rail (VSS or quite often ground). Instead of the load resistor of NMOS logic gates, CMOS logic gates have a collection of p-type MOSFETS in a pull up network between the output and the higher-voltage rail (often named Vdd) Thus if both a P-type and N-type transistor have their gates connected to the same input, the P-type MOSFET is OFF, and vice-versa. The network are arranged such that one is on and other OFF for any input pattern as shown in the figure 1. →

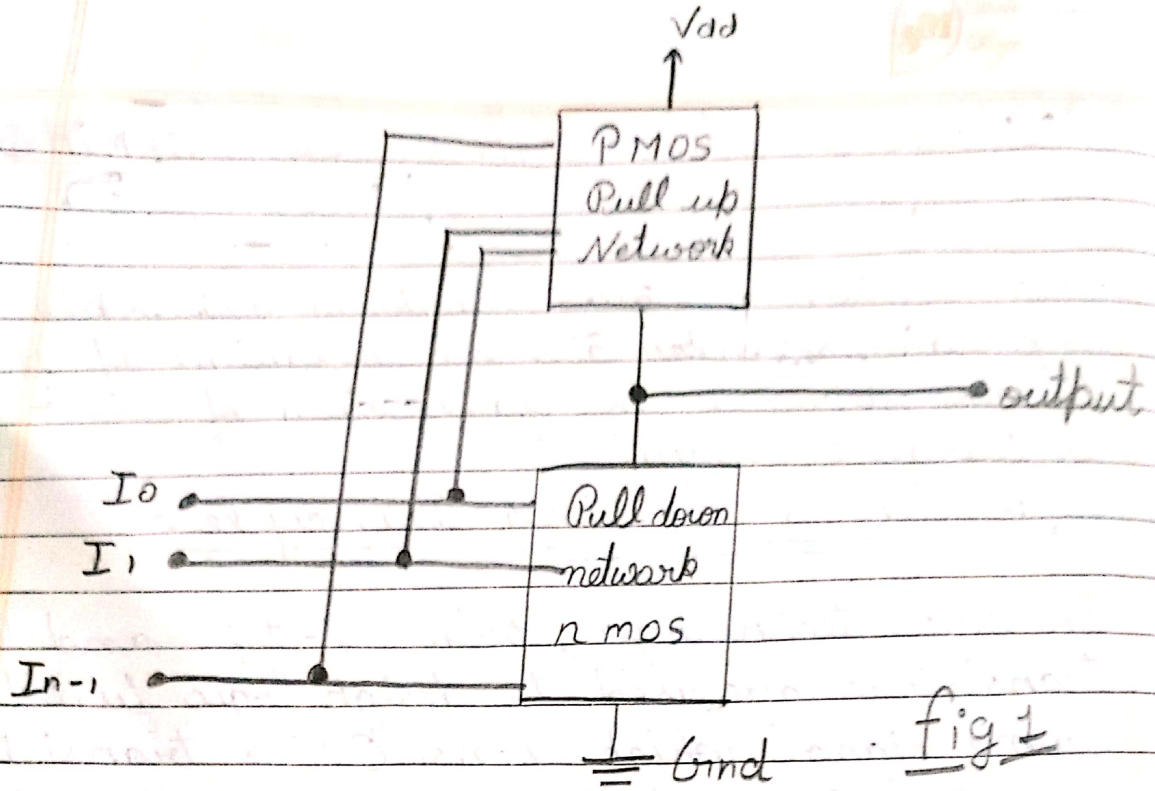
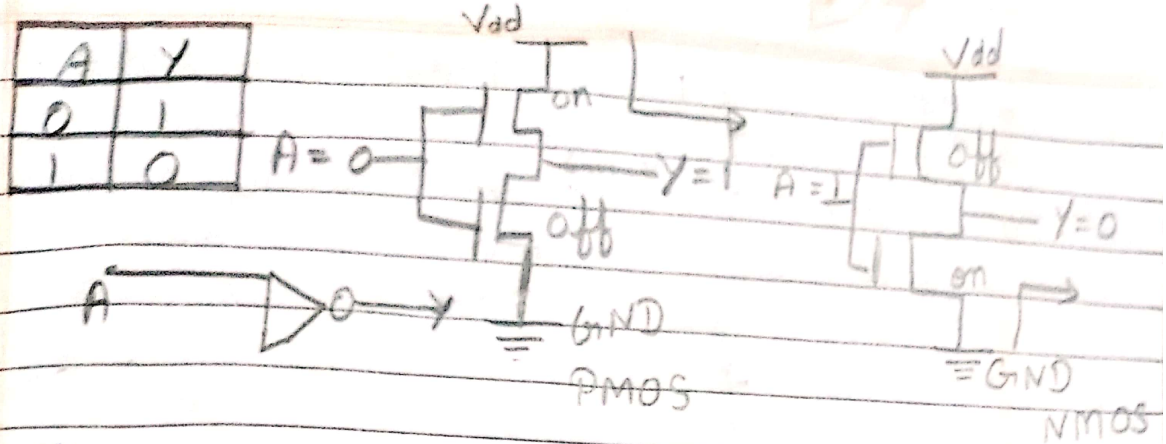


fig 1

CMOS offers relatively high speed, low power dissipation, high noise margincs in both states and will operate over a wide range of source and input voltage (provi the source voltage is fixed). Furthermore, for ~~this~~ the better understanding of the complementary metal oxide semiconductor working principle, we need to discuss in brief about CMOS logic gates as explained below.

CMOS Inverter:

The inverter circuits is shown in figure 2. It consists of PMOS and NMO FET. The input A serves as the gate volta for both transistors.



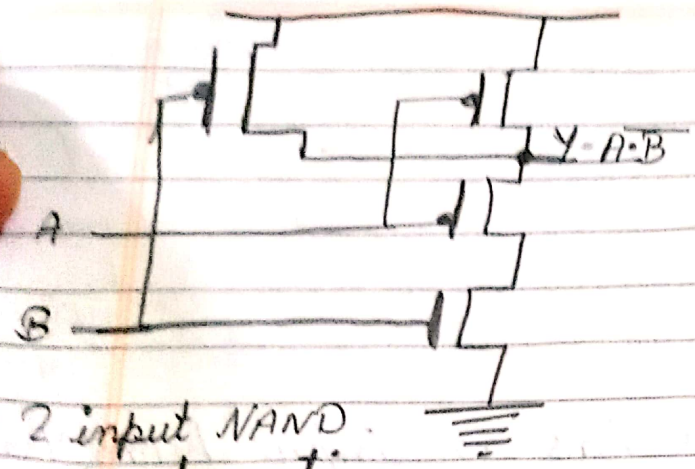
The NMOS transistor has an input from V_{ss} (ground) and PMOS transistor has an input from V_{dd}. The terminal Y is output. When a high voltage ($\sim V_{dd}$) is given at input terminal (A) of the inverter, the PMOS becomes open circuit and NMOS switched off so the output will be pulled down to V_{ss}.

When a low-level voltage ($< V_{dd}$, $\sim 0V$) applied to the inverter, the NMOS switched OFF and PMOS switched ON. So the output becomes V_{dd} or the circuit is pulled up to V_{dd}.

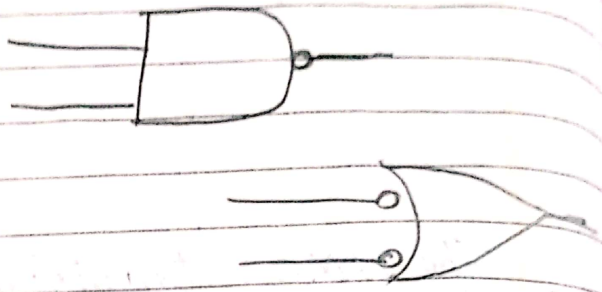
Input	Logic Input	Output	Logic
0V	0	Vdd	1
Vdd	1	0V	0

→ CMOS NAND Gate :-

The figure below shows a two input complementary MOS NAND gate. It consists of two series NMOS transistors between Y and Ground and two parallel PMOS transistors between Y and Vdd.



(a) 2 input NAND gate schematic



(b) NAND Gate symbol

If either input A or B is logic 0, at least one of the NMOS transistors will be off, breaking the path from Y to Ground. But at least one of the Pmos transistors will be ON, creating a path from Y to Vdd.

Hence, the output Y will be high.

If both inputs are high, both of the n-mos transistors will be ON and both of the P-mos transistors will be off.

Hence, the output will be logic low. The truth table of NAND logic gate given below:-

A	B	Pull-Down Network	Pull up Network	Output Y
0	0	Off	ON	1
0	1	Off	ON	1
1	0	Off	ON	1
1	1	Off	Off	0

CMOS NOR Gate :-

The two input NOR gate is shown in the figure below. The NMOS transistors are in parallel to pull the output low when either input is high. The PMOS transistors are in series to pull the output high when both inputs are low as in the table. The output is never left floating.

The truth table of NOR logic gate is given in below table :-

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

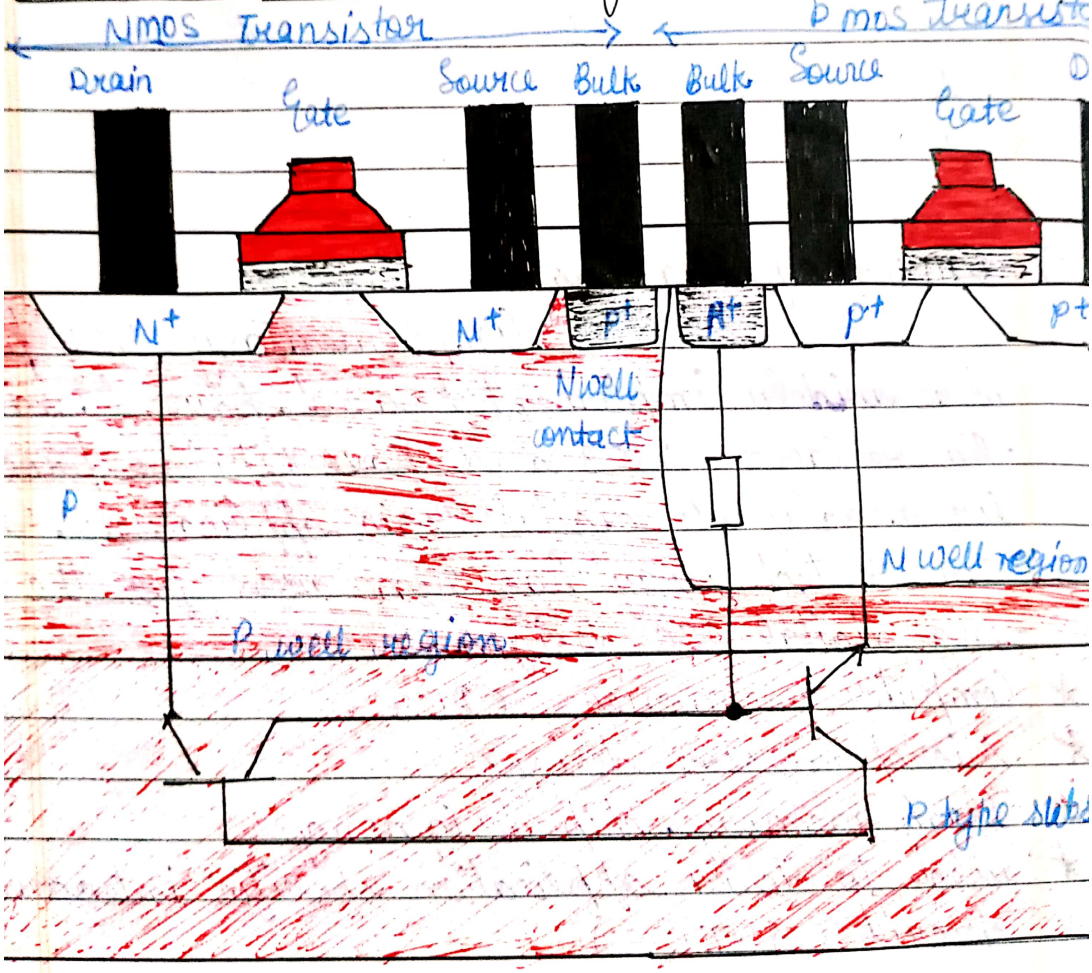
⇒ CMOS Applications :-

Complementary MOS proces
were widely implemented and have fundame
-lly replaced NMOS and Bipolar processe
for nearly all digital logic applications. The
CMOS technology has been used for the foll
-ing digital IC designs :-

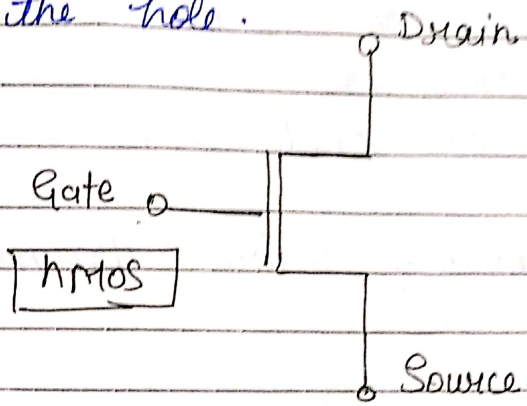
- ★ Computer memories, CPUS
- ★ Microprocessor designs
- ★ Flash memory, chip designing
- ★ used to design application specific integarated circuit (ASICS)

The main advantage of cmos over N mos and bipolar technology is the much smaller power dissipation. Unlike nmos or bipolars circuit a complementary mos circuit has almost not static power dissipation. Power is only dissipated in case the circuit actual switches. This allowes integrating more cmos gate on an IC than in NMOS or bipolar technology, resulting in much better performance. Complementary metal oxide semiconductor transistor consists of p-channel mos (PMOS) and N channel mos (NMOS

The fabrication Process of cmos Transistor :-



NMOS :- N MOS is built on a p-type substrate with n-type source and drain diffused on it. In NMOS, the majority charge carriers are electrons. When a high voltage is applied to the gate, the NMOS will conduct. Similarly, when a low voltage is applied to the gate, NMOS will not conduct. NMOS are considered to be faster than PMOS since the carrier in NMOS, which are electon, travel twice as fast as the hole.



PMOS :- P channel MOSFET consists P-type source and drain diffused on an N-type substrate. Majority carriers are holes. When a high voltage is applied to the gate, the PMO will not conduct. When a low voltage is applied to the gate, the PMOS will conduct. The PMOS devices are more immune to noise than NMOS devices.